

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

olicant

Catthoor, et al.

Group Art Unit 2151

App. No.

09/935,789

Filed

August 22, 2001

For

TASK CONCURRENCY

MANAGEMENT DESIGN

METHOD

Examiner

Unknown

RECEIVED

OCT 0 8 2003

Technology Center 2100

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Enclosed is form PTO-1449 listing 35 references that are also enclosed.

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required in accordance with 37 C.F.R. § 1.97(b)(3). If a first Office Action on the merits was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Eric M. Nelson

Registration No. 43,829

Attorney of Record

Customer No. 20,995 (619) 235-8550

S:\DOC\$\EMN\EMN-2924.DOC:sad:091103



RECEIVED,

OCT 0 8 2003

Case Docket No. IMEC218.001AUS

Date: October 1, 2003

Technology Center 2100

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants

Catthoor, et al.

Appl. No.

09/935,789

Filed

August 22, 2001

For

TASK CONCURRENCY MANAGEMENT DESIGN

METHOD

Examiner

Unknown

Group Art Unit:

2151

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

October 1, 2003

(Date)

Eric M. Nelson, Reg. No. 43,829

TRANSMITTAL LETTER

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application are:

- A Supplemental Information Disclosure Statement. (X)
- (X) A PTO Form 1449 with thirty-five (35) references.
- The Commissioner is hereby authorized to charge any additional fees which may be required, or (X) credit any overpayment, to Account No. 11-1410.
- (X) Return prepaid postcard.

Eric M. Nelson Registration No. 43,829 Attorney of Record Customer No. 20,995 (619) 235-8550

S:\DOCS\EMN\EMN-2925.DOC:sad 100103

TECHNOLOGY CENTER 2800

FORM (TO-1449

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE ATTY: DOCKET NO. IMEC218.001AUS

APPLICATION NO. 09/935,789

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT **BY APPLICANT**

E SEVERAL SHEETS IF NECESSARY)

APPLICANT

Catthoor, et al.

FILING DATE August 22, 2001 GROUP 2151

Technology Center 2100

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
	1	5,202,975	04/13/93	Rasbold et al.			
	2	5,327,561	07/05/94	Choi et al.			
· · ·	3	5,594,864	01/1997	Trauben	714	39	
	4	5,664,193	09/1997	Tirumalai	717	153	
	5	5,742,814	04/21/98	Balasa et al.			
	6	5,930,510	07/27/99	Beylin et al.		E C	
	7	5,978,509	11/1999	Nachtergaele et al.	382	236	0 70
	8	6,064,819	05/2000	Franssen et al.	717	156 🔓	ë c
	9	6,078,745	06/2000	De Greef et al.	717	151	E 29
	10	6,151,705	11/21/00	Santhanam		4	2) 2)

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
	11	Al-Furiah et al., "Memory Hierarchy Management for Interactive graph Structures", Proceedings, IEEE International Symposium on Parallel and Distributed Processing, March-April, 1998.
	12	Al-Mouhamed, M., et al., "A Heuristic Storage for Minimizing Access Time of Arbitrary Data Patterns", IEEE Transactions on Parallel and Distributed Systems, Vol. 8 No. 4, April 1997.
	13	Balasa, F., et al., "Dataflow-Driven Memory Allocation for Multi-Dimensional Signal Processing Systems", <i>Proceedings IEEE International Conference on Computer Aided Design</i> , San Jose, CA, pps. 31-34, Nov. 1994.
	14	Catthoor et al. "Global Communication and Memory Optimizing Transformations for Low Power Signal Processing Systems", IEEE workshop on VLSI signal processing, 1994.
	15	Catthoor et al., "System-Level Data-Flow Transformations for Power Reduction in Image and Video Processing", Proceedings of the Third IEEE International Conference on Electronics, Circuits and Systems, 1996.
	16	Catthoor, "Power-Efficient Data Storage and Transfer Methodologies: Current Solutions and Remaining Problems", IEEE Computer Society Workshop on VLSI System Level Design, 1998.
	17	Chen, Tien-Fu et al., "A Hierarchical Memory Directory Scheme via Extending SCI for Large Scale Multiprocessors", High Performance Computing on International Superhighway, April-May 1997.
	18	Danckaert et al., "System Level Memory Optimization for Hardware-Software Co-Design", Proceedings of the Fifth International Workshop on Hardware/Software Co-Design, 1997.
	19	De Greef, E., et al. "Mapping Real-Time Motion Estimation Type Algorithms to Memory Efficient, Programmable Multi- Processor Architectures, "Microprocessing and Microprogramming, 41(5): 409-423, October 1995.
	20	De Greef, E., F. Catthoor, H. De Man, "Memory Size Reduction Through Storage Order Optimization for Embedded Parallel Multimedia Applications", International Parallel Processing Symposium (IPPS) in Proceedings Workshop on Parallel Processing and Multimedia Geneva, Switzerland, pp. 84-98, April 1997.
	21	The state of the s

EXAMINER	ł
----------	---

DATE CONSIDERED

*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

FÖRM 3TO-1449

0 6 2003

OCT

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTY, DOCKET NO. IMEC218,001AUS

APPLICATION NO. 09/935,789

RECEIVED

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT

HE SEVERAL SHEETS IF NECESSARY)

APPLICANT Catthoor, et al.

OCT 8 8 2003

FiLING DATE August 22, 2001 GROUP 2151

Technology Center 2100

THE DE PARTY		
EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
	22	Fang, J., et al., "An Iteration Partition Approach for Cache or Local Memory Thrashing on Parallel Processing", IEEE Transactions on Computers, Vol. C-42, No 5, pp. 529-546, May 1993.
	23	Franssen et al., "Control Flow Optimization for Fast System Simulation and Storage Minimization", European Design and Test Conference, 1994.
	24	Li, YanBing et al., "A Task-Level Hierarchical Memory Model for System Synthesis of Multiprocessors", Proceedings, 34 th Design Automation Conference, June 1997.
	25	Lippens, P., et al, "Allocation of Multiport Memories for Hierarchical Data Streams", <i>Proceedings IEEE International Conference on Computer Aided Designs</i> , pps. 728-735, Santa Clara, Nov. 1993.
		Moolenaar, et al., "System-Level Power Exploration for MPEG-2 Decoder on Embedded Cores: A Systematic Approach", 1997 IEEE Workshop on Signal Processing Systems, 1997.
	27	Nachtergaele, L., F. Catthoor, F. Balasa, F. Franssen, E. De Greef, H. Samsom, H. De Man, "Optimization of Memory Organization and Hierarchy for Decreased Size and Power in Video and Image Processing Systems", Proceedings International Workshop on Memory Technology, Design and Testing, San Jose, CA, pp. 82-87, August 1995.
	28	Nachtergaele, L., F. Catthoor, B. Kapoor, D. Moolenaar, S., Janssen, "Low Power Storage Exploration for H.263 Video Decoder, IEEE Workshop on VLSI Signal Processing", Monterey, CA, pp. 114-124, Oct. 1996
	29	Pinter, S.S., "Register Allocation with Instruction Scheduling A New Approach", <i>ACM SIGPLAN Notices</i> , Vol. 28, pp. 248-257, June 1993.
	30	Sentieys, O., et al., "Memory Module Selection For High Level Synthesis", <i>Proceedings IEEE Workshop on VLSI Signal Processing, Monterey, CA</i> , pps. 272-283, Oct. 1996.
	31	Slock, P., S. Wuytack, F. Catthoor, G. De Jong, "Fast and Extensive System-Level Memory Exploration for ATM Application", Accepted for Proceedings 10 th ACM/IEEE International Symposium on System-Level Synthesis, Antwerp, Belgium, pp. 74-81, Sept. 1997
	32	Stok, L., "Data Path Synthesis", The VLSI Journal, Vol. 18, pp. 1-71, June 1994.
	33	Verhaegh, W., et al., "Improved Force-Directed Scheduling in High-Throughput Digital Signal Processing", IEEE Transactions on CAD and Systems, Vol. 14, No. 8, pps. 945-960, Aug. 1995.
	34	Wuytack, S., et al., "Flow Graph Balancing for Minimizing the Required Memory Bandwidth", <i>IEEE System Synthesis</i> , 1996 Proceedings, 9 th edition, 1996.
	35	Wuytack, S., F. Catthoor, L. Nachtergaele, H. De Man, "Power Exploration for Data Dominated Video Applications, Proceedings IEEE International Symposium on Low Power Design", Monterey, pp. 359-364, August 1996.

S:\DOCS\EMN\EMN-2923.DOC:sad4\pb 100103

RECEIVED

DEC 29 2003

TECHNOLOGY CENTER 2800

EXAMINER

DATE CONSIDERED